Claims

[c1] 1. A semiconductor structure, comprising:
(a) a semiconductor substrate; and
(b) N substructures on the substrate, N being a positive integer, each of the N substructures comprising:
(i) first and second FinFET active regions, wherein the first FinFET active region includes at least first and second devices, and
(ii) a back gate region abutting and being sandwiched between the first and second FinFET active regions, wherein the back gate region is shared by the first and second devices.

[c2] 2. The semiconductor structure of claim 1, wherein the second FinFET active region includes at least third and fourth devices, and wherein the back gate region is shared by the third and fourth devices.

[c3] 3. The semiconductor structure of claim 2, further comprising a first main gate region shared by the first and third devices.

[c4] 4. The semiconductor structure of claim 3, further comprising a second main gate region shared by the second

and fourth devices.

[c5] 5. The semiconductor structure of claim 1, wherein the first and second FinFET active regions comprise semiconductor devices of a same channel type.

[c6] 6. The semiconductor structure of claim 1, wherein the N substructures comprise M SRAM memory cells, M being a positive integer.

[c7] 7. The semiconductor structure of claim 1, wherein the N substructures comprise M logic circuits, M being a positive integer.

[c8] 8. The semiconductor structure of claim 1, wherein N > 1.

[c9] 9. A method for forming a semiconductor structure, the method comprising the steps of:
(a) providing a semiconductor region directly on an underlying electrically isolating layer, the semiconductor region being covered on top by a mandrel and a spacer;
(b) forming a back gate region separated from the semiconductor region by a back gate isolating layer and covered by an inter-gate isolating layer;
(c) removing a portion of the semiconductor region beneath the mandrel so as to form an active region adjacent to the removed portion of the semiconductor re-

gion; and

(d) forming a main gate region in place of the removed portion of the semiconductor region and on the inter-gate isolating layer, the main gate region being separated from the active region by a main gate isolating layer and being separated from the back gate region by the inter-gate isolating layer.

[c10] 10. The method of claim 9, wherein step (a) comprises:

forming the mandrel and the spacer on a top surface of a semiconductor layer; and

etching portions of the semiconductor layer not covered by the mandrel and the spacer.

[c11] 11. The method of claim 9, wherein step (b) comprises:

oxidizing an exposed-to-atmosphere surface of the semiconductor region to form the back gate isolating layer;

depositing a layer of a gate material on the underlying electrically isolating layer, the layer of the gate material being separated from the semiconductor region by the back gate isolating layer;

planarizing a top surface the layer of the gate material; and

oxidizing an exposed-to-atmosphere surface of the layer of the gate material to form the inter-gate isolating layer.

[c12] 12. The method of claim 9, wherein step (c) comprises:
removing the mandrel; and
etching the portion of the semiconductor region beneath the removed mandrel to form the active region.

[c13] 13. The method of claim 9, wherein step (d) comprises:
oxidizing an exposed-to-atmosphere surface of the active region so as to form the main gate isolating layer; and
depositing a layer of a gate material in place of the removed portion of the semiconductor region and on the inter-gate isolating layer so as to form the main gate region.

[c14] 14. The method of claim 9, wherein an interfacing surface between the main gate isolating layer and the active region is substantially perpendicular to a top surface of the structure.

[c15] 15. The method of claim 9, wherein an interfacing surface between the back gate isolating layer and the active region is substantially perpendicular to a top surface of the structure.

[c16] 16. The method of claim 9, wherein the mandrel comprises silicon nitride.

[c17] 17. A method for forming a semiconductor structure, the method comprising:
providing a substrate with an isolating layer including a semiconductor layer directly on top of an underlying electrically isolating layer;
forming a mandrel and first and second spacers on top of the semiconductor layer, the mandrel being sandwiched between the first and second spacers;
etching portions of the semiconductor layer not covered by the mandrel and the first and second spacers;
forming a back gate isolating layer on exposed surfaces of the semiconductor layer;
depositing a gate material on the structure and planarizing a top surface of the structure such that the mandrel is exposed;
selectively forming an inter-gate insulating layer on the gate material such that the mandrel is still exposed to the atmosphere;
removing the mandrel;
etching the semiconductor layer under the removed mandrel so as to form first and second active regions being aligned with the first and second spacers, respectively;
forming a dielectric layer on exposed surfaces of the gate material; and
depositing the gate material on the structure so as to

form a main gate region.

[c18] 18. The method of claim 17, wherein the step of forming the back gate isolating layer on exposed surfaces of the semiconductor layer comprises the step of thermally oxidizing the exposed surfaces of the semiconductor layer.

[c19] 19. The method of claim 17, wherein the gate material comprises polysilicon.

[c20] 20. The method of claim 17, wherein the step of selectively forming the inter-gate insulating layer comprises the step of thermally oxidizing exposed surfaces of the gate material.